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What is claimed is :

1. A detector for detecting at least one kind of dependence in address between instructions executed by at least a processor, said detector  
5 being adopted to detect a possibility of presence of said at least one kind of dependence,

wherein if said at least one kind of dependence is present in fact, then said detector detects a possibility of presence of said at least one kind of dependence, and if said at least one kind of dependence is not present in  
10 fact, then said detector is allowed to detect said at least one kind of dependence.

2. The detector as claimed in claim 1, wherein said instruction comprises a memory access instruction for access to a memory.  
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3. The detector as claimed in claim 2, wherein said detector includes :

an execution history storing unit including a plurality of entry which stores an instruction execution information of whether said memory  
20 access instruction has been executed ; and

an address converter for converting an address of said memory access instruction into an entry number of said entry of said execution history storing unit,

so that said execution history storing unit stores said instruction

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execution information into said entry designated by said entry number.

4. The detector as claimed in claim 3, wherein said address converter is adopted to convert a same address of different memory access instructions into a same entry number for allowing that the same address for said different memory access instructions is stored in the same entry, whereby if said at least one kind of dependence is not present in fact, then said detector is adopted to detect said at least one kind of dependence.

10 5. The detector as claimed in claim 4, wherein said memory access instruction comprises either a load instruction or a store instruction.

6. The detector as claimed in claim 5, wherein said one kind of said dependence is a read after write dependence, and  
15 if said load instruction has been executed, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector stores an instruction execution information, that said load instruction has been executed, into said entry designated by said entry number of said execution history storing unit, and

20 if said store instruction has been executed, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said load instruction has been executed, out from said entry designated by said entry number of said execution history storing unit,

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whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed into said load instruction as executed.

- 5 7. The detector as claimed in claim 5, wherein said one kind of said dependence is a write after read dependence, and

if said store instruction has been executed, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector stores an instruction execution information,  
10 that said store instruction has been executed, into said entry designated by said entry number of said execution history storing unit, and

if said load instruction has been executed, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector reads an instruction execution information,  
15 whether or not said store instruction has been executed, out from said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said write after read dependence from said load instruction as executed into said store instruction as executed.

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8. The detector as claimed in claim 5, wherein said one kind of said dependence is a write after write dependence, and

if said store instruction has been executed, then said address converter is adopted to convert an address of said store instruction into an

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entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed, out from said entry designated by said entry number of said execution history storing unit, and also said detector stores an instruction execution information, that said store instruction has been executed, into said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said write after write dependence between said store instructions as executed.

9. The detector as claimed in claim 5, wherein said one kind of said dependence is a read after write dependence, a write after read dependence and an write after write dependence and

- if said load instruction has been executed, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed, from said entry designated by said entry number of said execution history storing unit, and also said detector stores an instruction execution information, that said load instruction has been executed, into said entry designated by said entry number of said execution history storing unit, and

if said store instruction has been executed, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads instruction execution informations, whether or not said load instruction has been executed and whether or not

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said store instruction has been executed, out from said entry designated by said entry number of said execution history storing unit, and also said detector stores an instruction execution information, that said store instruction has been executed into said entry designated by said entry  
5 number of said execution history storing unit,

whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed into said load instruction as executed, and also detects a possibility of presence of said write after read dependence from said load instruction as executed  
10 into said store instruction as executed as well as detects a possibility of presence of said write after write dependence between said store instructions as executed.

10. The detector as claimed in claim 4, wherein said address converter is adopted to select plural bits of said address inputted and output said plural bits as indicating said entry number.  
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11. The detector as claimed in claim 10, wherein said address converter is adopted to take an exclusive-OR of said selected plural bits and output a value of said exclusive-OR as indicating said entry number.  
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12. A detector provided in a self-processor included in a multiple processor system including said self-processor and at least a processor other than said self-processor, and said multiple processor system

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performing parallel processings in thread units of program, and said detector detecting at least one kind of dependence in address between an instruction included in a thread executed by said self-processor and an instruction included in a thread executed by said other processor, said  
5 detector being adopted to detect a possibility of presence of said at least one kind of dependence,

wherein if said at least one kind of dependence is present in fact, then said detector detects a possibility of presence of said at least one kind of dependence, and if said at least one kind of dependence is not present in  
10 fact, then said detector is allowed to detect said at least one kind of dependence.

13. The detector as claimed in claim 12, wherein said instruction comprises a memory access instruction for access to a memory.

14. The detector as claimed in claim 13, wherein said detector includes :

an execution history storing unit including a plurality of entry which stores an instruction execution information of whether said memory  
20 access instruction has been executed ; and

an address converter for converting an address of said memory access instruction into an entry number of said entry of said execution history storing unit,

so that said execution history storing unit stores said instruction

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execution information into said entry designated by said entry number.

15. The detector as claimed in claim 14, wherein said address converter is adopted to convert a same address of different memory access instructions into a same entry number for allowing that the same address for said different memory access instructions is stored in the same entry, whereby if said at least one kind of dependence is not present in fact, then said detector is adopted to detect said at least one kind of dependence.

16. The detector as claimed in claim 15, wherein only if said memory access instruction has been executed by other processor than said self-processor, and said other processor is to execute a thread which is prior in program sequence to said thread executed by said self-processor, then said address converter is adopted to convert an address of said memory access instruction into an entry number of said entry, and said detector reads an instruction execution information, whether or not said memory accesses instruction has been executed, from an entry designated by said entry number.

17. The detector as claimed in claim 15, wherein if said memory access instruction has been executed by other processor than said self-processor, then said address converter is adopted to convert an address of said memory access instruction into an entry number of said entry, and said detector reads an instruction execution information, whether or not said

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memory accesses instruction has been executed, from an entry designated by said entry number by referring only a value which has been read out by said memory access instruction which had been executed by other processor executing a thread which is prior in program sequence to said thread executed by said self-processor.

18. The detector as claimed in claim 15, wherein said memory access instruction comprises either a load instruction or a store instruction.

19. The detector as claimed in claim 18, wherein said one kind of said dependence is a read after write dependence, and

if said load instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector stores an instruction execution information, that said load instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit, and

if said store instruction has been executed by said other processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said load instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said



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read after write dependence from said store instruction as executed by said other processor into said load instruction as executed by said self-processor.

20. The detector as claimed in claim 18, wherein said one kind of  
5 said dependence is a write after read dependence, and

if said store instruction has been executed by said self-processor,  
then said address converter is adopted to convert an address of said store  
instruction into an entry number, and said detector stores an instruction  
execution information, that said store instruction has been executed by said  
10 self-processor, into said entry designated by said entry number of said  
execution history storing unit, and

if said load instruction has been executed by said other processor,  
then said address converter is adopted to convert an address of said load  
instruction into an entry number, and said detector reads an instruction  
15 execution information, whether or not said store instruction has been  
executed by said self-processor, out from said entry designated by said  
entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said  
write after read dependence from said load instruction as executed by said  
20 other processor into said store instruction as executed by said self-processor.

21. The detector as claimed in claim 18, wherein said one kind of  
said dependence is a write after write dependence, and

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if said store instruction has been executed by said other processor,  
then said address converter is adopted to convert an address of said store  
instruction into an entry number, and said detector reads an instruction  
execution information, whether or not said store instruction has been  
5 executed by said self-processor, out from said entry designated by said  
entry number of said execution history storing unit,

if said store instruction has been executed by said self-processor,  
then said address converter is adopted to convert an address of said store  
instruction into an entry number, and said detector stores an instruction  
10 execution information, that said store instruction has been executed by said  
self-processor, into said entry designated by said entry number of said  
execution history storing unit,

whereby said detector detects a possibility of presence of said  
write after write dependence from said store instruction as executed by said  
15 other processor to said store instruction as executed by said self-processor.

22. The detector as claimed in claim 18, wherein said one kind of  
said dependence is a read after write dependence, a write after read  
dependence and an write after write dependence and

20 if said load instruction has been executed by said other processor,  
then said address converter is adopted to convert an address of said load  
instruction into an entry number, and said detector reads an instruction  
execution information, whether or not said store instruction has been  
executed by said self-processor, from said entry designated by said entry

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number of said execution history storing unit,

if said store instruction has been executed by said other processor,  
then said address converter is adopted to convert an address of said store  
instruction into an entry number, and said detector reads an instruction  
5 execution information, whether or not said load instruction has been  
executed by said self-processor, from said entry designated by said entry  
number of said execution history storing unit,

if said load instruction has been executed by said self-processor,  
then said address converter is adopted to convert an address of said load  
10 instruction into an entry number, and said detector stores an instruction  
execution information, that said load instruction has been executed by said  
self-processor, into said entry designated by said entry number of said  
execution history storing unit,

if said store instruction has been executed by said self-processor,  
15 then said address converter is adopted to convert an address of said store  
instruction into an entry number, and said detector stores an instruction  
execution information, that said store instruction has been executed by said  
self-processor, into said entry designated by said entry number of said  
execution history storing unit,

20 whereby said detector detects a possibility of presence of said  
read after write dependence from said store instruction as executed by said  
other processor into said load instruction as executed by said self-processor,  
and also detects a possibility of presence of said write after read  
dependence from said load instruction as executed by said other processor

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into said store instruction as executed by said self-processor as well as detects a possibility of presence of said write after write dependence from said store instruction as executed by said other processor into said store instruction as executed by said self-processor.

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23. The detector as claimed in claim 13, wherein said address converter is adopted to select plural bits of said address inputted and output said plural bits as indicating said entry number.

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24. The detector as claimed in claim 23, wherein said address converter is adopted to take an exclusive-OR of said selected plural bits and output a value of said exclusive-OR as indicating said entry number.

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25. A detector provided in a self-processor included in a multiple processor system including said self-processor and at least a processor other than said self-processor, and said multiple processor system performing parallel processings in thread units of program, and said detector detecting at least one kind of dependence in address between an instruction included in a thread executed by said self-processor and an instruction included in a thread executed by said other processor, said detector being adopted to detect a possibility of presence of said at least one kind of dependence, as well as said detector detecting at least one kind of dependence in address between instructions included in a thread executed by said self-processor,

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wherein if said at least one kind of dependence is present in fact,  
then said detector detects a possibility of presence of said at least one kind  
of dependence, and if said at least one kind of dependence is not present in  
fact, then said detector is allowed to detect said at least one kind of  
5 dependence.

26. The detector as claimed in claim 25, wherein said instruction  
comprises a memory access instruction for access to a memory.

10 27. The detector as claimed in claim 26, wherein said detector  
includes :

an execution history storing unit including a plurality of entry  
which stores an instruction execution information of whether said memory  
access instruction has been executed ; and

15 an address converter for converting an address of said memory  
access instruction into an entry number of said entry of said execution  
history storing unit,

so that said execution history storing unit stores said instruction  
execution information into said entry designated by said entry number.

20 28. The detector as claimed in claim 27, wherein said address  
converter is adopted to convert a same address of different memory access  
instructions into a same entry number for allowing that the same address  
for said different memory access instructions is stored in the same entry,

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whereby if said at least one kind of dependence is not present in fact, then said detector is adopted to detect said at least one kind of dependence.

29. The detector as claimed in claim 28, wherein only if said  
5 memory access instruction has been executed by other processor than said self-processor, and said other processor is to execute a thread which is prior in program sequence to said thread executed by said self-processor, then said address converter is adopted to convert an address of said memory access instruction into an entry number of said entry, and said detector  
10 reads an instruction execution information, whether or not said memory accesses instruction has been executed, from an entry designated by said entry number.

30. The detector as claimed in claim 28, wherein if said memory  
15 access instruction has been executed by other processor than said self-processor, then said address converter is adopted to convert an address of said memory access instruction into an entry number of said entry, and said detector reads an instruction execution information, whether or not said memory accesses instruction has been executed, from an entry designated  
20 by said entry number by referring only a value which has been read out by said memory access instruction which had been executed by other processor executing a thread which is prior in program sequence to said thread executed by said self-processor.

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31. The detector as claimed in claim 30, wherein said one kind of said dependence is a read after write dependence, and said memory access instruction comprises either a load instruction or a store instruction,

if said load instruction has been executed by said self-processor,  
5 then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector stores an instruction execution information, that said load instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit, and

10 if said store instruction has been executed by either said self-processor or said other processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said load instruction has been executed by said self-processor, out from said  
15 entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed by either said self-processor or said other processor into said load instruction  
20 as executed by said self-processor.

32. The detector as claimed in claim 30, wherein said one kind of said dependence is a write after read dependence, and said memory access instruction comprises either a load instruction or a store instruction,

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if said store instruction has been executed by said self-processor,  
then said address converter is adopted to convert an address of said store  
instruction into an entry number, and said detector stores an instruction  
execution information, that said store instruction has been executed by said  
5 self-processor, into said entry designated by said entry number of said  
execution history storing unit, and

if said load instruction has been executed by either said self-  
processor or said other processor, then said address converter is adopted to  
convert an address of said load instruction into an entry number, and said  
10 detector reads an instruction execution information, whether or not said  
store instruction has been executed by said self-processor, out from said  
entry designated by said entry number of said execution history storing  
unit,

whereby said detector detects a possibility of presence of said  
15 write after read dependence from said load instruction as executed by either  
said self-processor or said other processor into said store instruction as  
executed by said self-processor.

33. The detector as claimed in claim 30, wherein said one kind of  
20 said dependence is an write after write dependence, and said memory  
access instruction comprises either a load instruction or a store instruction,

if said store instruction has been executed by said other processor,  
then said address converter is adopted to convert an address of said store  
instruction into an entry number, and said detector reads an instruction



execution information, whether or not said store instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit,

if said store instruction has been executed by said self-processor,  
5 then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit, as well as said detector  
10 stores an instruction execution information, that said store instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said write after write dependence from said store instruction as executed by  
15 either said self-processor or said other processor to said store instruction as executed by said self-processor.

34. The detector as claimed in claim 30, wherein said one kind of said dependence is a read after write dependence, a write after read  
20 dependence and an write after write dependence, and said memory access instruction comprises either a load instruction or a store instruction,

if said load instruction has been executed by either said self-processor or said other processor, then said address converter is adopted to convert an address of said load instruction into an entry number, and said

detector reads an instruction execution information, whether or not said store instruction has been executed by said self-processor, from said entry designated by said entry number of said execution history storing unit,

if said store instruction has been executed by either said self-processor or said other processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said load instruction has been executed by said self-processor, from said entry designated by said entry number of said execution history storing unit,

if said load instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector stores an instruction execution information, that said load instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit,

if said store instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector stores an instruction execution information, that said store instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed by either said self-processor or said other processor into said load instruction

as executed by said self-processor, and also detects a possibility of presence of said write after read dependence from said load instruction as executed by either said self-processor or said other processor into said store instruction as executed by said self-processor as well as detects a possibility of presence of said write after write dependence from said store instruction as executed by either said self-processor or said other processor into said store instruction as executed by said self-processor.

35. The detector as claimed in claim 26, wherein said address converter is adopted to select plural bits of said address inputted and output said plural bits as indicating said entry number.

36. The detector as claimed in claim 35, wherein said address converter is adopted to take an exclusive-OR of said selected plural bits and output a value of said exclusive-OR as indicating said entry number.

37. A processor including :  
an instruction execution unit ;  
a processor control unit ; and  
a data dependence detector,  
wherein for allowing said processor to execute said instructions, said processor control unit supplies a kind of said instruction to said instruction execution unit and said data dependence detector, and if said instruction to be executed is a memory access instruction which comprises

either a load instruction for transferring data from a memory to a register or a store instruction for transferring data from said register to said memory, then said processor control unit supplies an address of said memory access instruction to said instruction execution unit and said data dependence detector as well as said processor control unit supplies said data dependence detector with a speculative execution flag which indicates that said memory access instruction is to be executed by a data dependence speculative execution, and

said data dependence detector further includes :

an execution history storing unit including a plurality of entry which stores an instruction execution information of whether said memory access instruction has been executed ; and

an address converter for converting an address of said memory access instruction into an entry number of said entry of said execution history storing unit, so that said execution history storing unit refers said speculative execution flag and an execution instruction from said processor control unit, and allows read/write operation of said instruction execution information to said entry designated by said entry number, and

said data dependence detector supplies said processor control unit with a value which indicates whether said data dependence execution has been in success or failure.

38. The processor as claimed in claim 37, wherein said address converter is adopted to convert a same address of different memory access

instructions into a same entry number for allowing that the same address for said different memory access instructions is stored in the same entry, whereby if said at least one kind of dependence is not present in fact, then said detector is adopted to detect said at least one kind of dependence.

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39. The processor as claimed in claim 38, wherein said address converter is adopted to select plural bits of said address inputted and output said plural bits as indicating said entry number.

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40. The processor as claimed in claim 39, wherein said address converter is adopted to take an exclusive-OR of said selected plural bits and output a value of said exclusive-OR as indicating said entry number.

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41. The processor as claimed in claim 37, wherein in case that said processor is in a state of a speculative instruction execution to said data dependence, and

if said processor has speculatively executed said load instruction, then said address converter converts said address of said load instruction into an entry number which is inputted into said instruction history storing unit, and

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said instruction history storing unit stores a value, which indicates that said load instruction has speculatively executed, into an entry designated by said entry number, and

if said processor has speculatively executed said store instruction,

then said address converter converts said address of said store instruction into an entry number which is inputted into said instruction history storing unit, and

5       said instruction history storing unit reads a stored value out from an entry designated by said entry number,

10       whereby said data dependence detector detects, based on said read out value, a possibility of presence of a read after write dependence from said store instruction from said load instruction, and if said possibility of presence of said read after write dependence is detected, said data dependence detector supplies said processor control unit with a value which indicates that said data dependence speculative execution has been in failure.

15       42.       The processor as claimed in claim 40, wherein said data dependence detector initializes all of said entries of said instruction history storing unit based on said speculative execution flag.

20       43.       The processor as claimed in claim 40, wherein if said data dependence detector supplies said processor control unit with a value which indicates that said data dependence speculative execution has been in failure, said processor control unit and said instruction execution unit perform a recovery process for failure of said data dependence speculative execution.

44. The processor as claimed in claim 40, wherein if no presence of said read after write dependence from said store instruction to said load instruction is detected, then said data dependence detector supplies said processor control unit with a value which indicates that said data  
5 dependence speculative execution has been in success, said processor control unit continues subsequent instruction executions without execution of a recovery process.

45. A multiple processor system for thread parallel processings, said  
10 system including :

a plurality of processor which further includes an instruction execution unit ; a processor control unit ; and a data dependence detector ;  
and

a thread control unit being adopted to allocate threads to said  
15 plurality of processor for allowing each of said plurality of processor to execute at least an allocated thread, and said thread control unit being also adopted to supply each of said plurality of processor with both a respective speculative execution flag which indicate whether or not said thread should be executed by a data dependence speculative execution, and a thread  
20 sequence which indicates execution sequences of said threads, whereby each of said processors receives said speculative execution flag and said thread sequences and executes said at least allocated thread allocated by said thread control unit,

wherein said processor control unit supplies a kind of an

instruction to be executed by a self-processor, in which said processor control unit is provided, to said instruction execution unit and said data dependence detector which are provided in said self-processor, and as well as to at least a processor other than said self-processor,

5           said data dependence detector receives said kind of said instruction to be executed by said self-processor, and also receives kinds of instructions to be executed by said other processor from processor control units provided in said other processor ;

10           if said instruction to be executed is either a load instruction or a store instruction, said processor control unit supplies an address of said instruction to said instruction execution unit and said data dependence detector which are provided in said self-processor, and as well as to said other processor ;

15           said data dependence detector includes the same number of address converter as a total number of said processors included in said system, an instruction history storing unit and a logic circuit ;

          said data dependence detector judges whether said self-processor is in a definitive execution state or a speculative execution state based on said speculative execution flag supplied from said thread control unit ;

20           said data dependence detector judges, whether said thread executed by said self-processor is prior in program sequence to a respective thread executed by said other processor, based on said thread sequences, and said data dependence detector supplies a data dependence detected result to said thread control unit ;



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one of said address converters converts an address of a load instruction to be executed by said self-processor into an entry number of said instruction history storing unit, and remaining of said address converters converts an address of a store instruction to be executed by said other processor into an entry number of said instruction history storing unit ;

said instruction history storing unit comprises a plurality of entry, a single write port and plural read ports which number is smaller by one than said total number of said processors ;

said address converter, which has an input port for receiving said address of said instruction to be executed by said self-processor, has an output port connected to said write port of said instruction history storing unit for write operation into an entry designated by said entry number of said instruction history storing unit ;

said address converter, which has an input port for receiving said address of said instruction to be executed by said other processor, has an output port connected to said read port of said instruction history storing unit for read operation from an entry designated by said entry number of said instruction history storing unit ; and

said logic circuit operates a logical-OR of said plural read ports of said address converter and supplies an operated logic value as a data dependence detected result to said thread control unit.

The system as claimed in claim 45, wherein said data dependence

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detector initializes all of said entries of said instruction history storing unit based on said speculative execution flag.

47. The system as claimed in claim 45, wherein if said self-processor  
5 is in said speculative execution state and said load instruction has  
speculatively been executed by said self-processor, then said address  
converter in said data dependence detector converts an address of said load  
instruction into an entry number of said instruction history storing unit and  
10 supplies said entry number to said write port of said instruction history  
storing unit, so that said instruction history storing unit sets a value  
indicating, that said load instruction has speculatively been executed, at an  
entry designated by said entry number,

if said self-processor is in said speculative execution state and  
said store instruction has been executed by other processor which is  
15 allocated with a prior thread which is prior in program sequence to a thread  
executed by said self-processor, then said address converter in said data  
dependence detector converts an address of said store instruction into an  
entry number of said instruction history storing unit and supplies said entry  
number to corresponding one of said input ports of said instruction history  
20 storing unit, so that said instruction history storing unit reads a content  
from an entry designated by said entry number and supplies said content to  
said logic circuit,

said logic circuit operates a logical-OR of said plural read ports  
of said address converter and supplies an operated logic value as a data

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dependence detected result to said thread control unit.

48. The system as claimed in claim 45, wherein if an address of a store instruction executed by other processor allocated with a prior thread which is prior in program sequence to a thread executed by said self-processor is either equal to an address of a load instruction subjected to a data dependence speculative execution by said self-processor or allocated to the same entry of said instruction history storing unit due to appearance of areas, then a value indicating, that said load instruction subjected to the data dependence speculative execution is present, is read out from said instruction history storing unit, a possibility of presence of a read after write dependence is detected, and said data dependence detector supplies a value indicating failure of said data dependence speculative execution to said thread control unit,

said thread control unit receives a notice of failure of said data dependence speculative execution from either one of said processors, and said thread control unit sends a request for recovery process against failure of said data dependence speculative execution to a processor which has supplied said notice of failure of said data dependence speculative execution as well as to a processor executing a thread which is post in program sequence to a thread executed by said processor which has supplied said notice, and

said processor control unit of said processor receives said request for said recovery process to failure of said data dependence speculative

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execution.

49. A semiconductor integrated circuit including a detector for detecting at least one kind of dependence in address between instructions executed by at least a processor, said detector being adopted to detect a possibility of presence of said at least one kind of dependence,

wherein if said at least one kind of dependence is present in fact, then said detector detects a possibility of presence of said at least one kind of dependence, and if said at least one kind of dependence is not present in fact, then said detector is allowed to detect said at least one kind of dependence.

50. The semiconductor integrated circuit as claimed in claim 49, wherein said instruction comprises a memory access instruction for access to a memory.

51. The semiconductor integrated circuit as claimed in claim 50, wherein said detector includes :

an execution history storing unit including a plurality of entry which stores an instruction execution information of whether said memory access instruction has been executed ; and

an address converter for converting an address of said memory access instruction into an entry number of said entry of said execution history storing unit,

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so that said execution history storing unit stores said instruction execution information into said entry designated by said entry number.

52. The semiconductor integrated circuit as claimed in claim 51,  
5 wherein said address converter is adopted to convert a same address of different memory access instructions into a same entry number for allowing that the same address for said different memory access instructions is stored in the same entry, whereby if said at least one kind of dependence is not present in fact, then said detector is adopted to detect said at least one  
10 kind of dependence.

53. The semiconductor integrated circuit as claimed in claim 52,  
wherein said memory access instruction comprises either a load instruction or a store instruction.

15 54. The semiconductor integrated circuit as claimed in claim 53,  
wherein said one kind of said dependence is a read after write dependence, and

if said load instruction has been executed, then said address  
20 converter is adopted to convert an address of said load instruction into an entry number, and said detector stores an instruction execution information, that said load instruction has been executed, into said entry designated by said entry number of said execution history storing unit, and

if said store instruction has been executed, then said address

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converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said load instruction has been executed, out from said entry designated by said entry number of said execution history storing unit,

5           whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed into said load instruction as executed.

55.       The semiconductor integrated circuit as claimed in claim 53,  
10       wherein said one kind of said dependence is a write after read dependence, and

          if said store instruction has been executed, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector stores an instruction execution information,  
15       that said store instruction has been executed, into said entry designated by said entry number of said execution history storing unit, and

          if said load instruction has been executed, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector reads an instruction execution information,  
20       whether or not said store instruction has been executed, out from said entry designated by said entry number of said execution history storing unit,

          whereby said detector detects a possibility of presence of said write after read dependence from said load instruction as executed into said store instruction as executed.

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56. The semiconductor integrated circuit as claimed in claim 53, wherein said one kind of said dependence is a write after write dependence, and

5 if said store instruction has been executed, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed, out from said entry designated by said entry number of said execution history storing unit, and  
10 also said detector stores an instruction execution information, that said store instruction has been executed, into said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said write after write dependence between said store instructions as executed.

15 57. The semiconductor integrated circuit as claimed in claim 53, wherein said one kind of said dependence is a read after write dependence, a write after read dependence and a write after write dependence and

20 if said load instruction has been executed, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed, from said entry designated by said entry number of said execution history storing unit, and also said detector stores an instruction execution information, that said load

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instruction has been executed, into said entry designated by said entry number of said execution history storing unit, and

if said store instruction has been executed, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads instruction execution informations, whether or not said load instruction has been executed and whether or not said store instruction has been executed, out from said entry designated by said entry number of said execution history storing unit, and also said detector stores an instruction execution information, that said store instruction has been executed into said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed into said load instruction as executed, and also detects a possibility of presence of said write after read dependence from said load instruction as executed into said store instruction as executed as well as detects a possibility of presence of said write after write dependence between said store instructions as executed.

58. The semiconductor integrated circuit as claimed in claim 52, wherein said address converter is adopted to select plural bits of said address inputted and output said plural bits as indicating said entry number.

59. The semiconductor integrated circuit as claimed in claim 58,



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wherein said address converter is adopted to take an exclusive-OR of said selected plural bits and output a value of said exclusive-OR as indicating said entry number.

- 5 60. A semiconductor integrated circuit including a detector provided in a self-processor included in a multiple processor system including said self-processor and at least a processor other than said self-processor, and said multiple processor system performing parallel processings in thread units of program, and said detector detecting at least one kind of  
10 dependence in address between an instruction included in a thread executed by said self-processor and an instruction included in a thread executed by said other processor, said detector being adopted to detect a possibility of presence of said at least one kind of dependence,

- 15 wherein if said at least one kind of dependence is present in fact, then said detector detects a possibility of presence of said at least one kind of dependence, and if said at least one kind of dependence is not present in fact, then said detector is allowed to detect said at least one kind of dependence.

- 20 61. The semiconductor integrated circuit as claimed in claim 60, wherein said instruction comprises a memory access instruction for access to a memory.

62. The semiconductor integrated circuit as claimed in claim 61,

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wherein said detector includes :

an execution history storing unit including a plurality of entry which stores an instruction execution information of whether said memory access instruction has been executed ; and

5 an address converter for converting an address of said memory access instruction into an entry number of said entry of said execution history storing unit,

so that said execution history storing unit stores said instruction execution information into said entry designated by said entry number.

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63. The semiconductor integrated circuit as claimed in claim 62, wherein said address converter is adopted to convert a same address of different memory access instructions into a same entry number for allowing that the same address for said different memory access instructions is stored in the same entry, whereby if said at least one kind of dependence is not present in fact, then said detector is adopted to detect said at least one kind of dependence.

15

64. The semiconductor integrated circuit as claimed in claim 63, wherein only if said memory access instruction has been executed by other processor than said self-processor, and said other processor is to execute a thread which is prior in program sequence to said thread executed by said self-processor, then said address converter is adopted to convert an address of said memory access instruction into an entry number of said entry, and

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said detector reads an instruction execution information, whether or not said memory accesses instruction has been executed, from an entry designated by said entry number.

5 65. The semiconductor integrated circuit as claimed in claim 63, wherein if said memory access instruction has been executed by other processor than said self-processor, then said address converter is adopted to convert an address of said memory access instruction into an entry number of said entry, and said detector reads an instruction execution information,  
10 whether or not said memory accesses instruction has been executed, from an entry designated by said entry number by referring only a value which has been read out by said memory access instruction which had been executed by other processor executing a thread which is prior in program sequence to said thread executed by said self-processor.

15 66. The semiconductor integrated circuit as claimed in claim 63, wherein said memory access instruction comprises either a load instruction or a store instruction.

20 67. The semiconductor integrated circuit as claimed in claim 66, wherein said one kind of said dependence is a read after write dependence, and

if said load instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said load

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instruction into an entry number, and said detector stores an instruction execution information, that said load instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit, and

- 5 if said store instruction has been executed by said other processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said load instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed by said other processor into said load instruction as executed by said self-processor.

- 15 68. The semiconductor integrated circuit as claimed in claim 66, wherein said one kind of said dependence is a write after read dependence, and

if said store instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector stores an instruction execution information, that said store instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit, and

if said load instruction has been executed by said other processor,

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then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said write after read dependence from said load instruction as executed by said other processor into said store instruction as executed by said self-processor.

69. The semiconductor integrated circuit as claimed in claim 66, wherein said one kind of said dependence is an write after write dependence, and

if said store instruction has been executed by said other processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit,

if said store instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector stores an instruction execution information, that said store instruction has been executed by said self-processor, into said entry designated by said entry number of said

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execution history storing unit,

whereby said detector detects a possibility of presence of said write after write dependence from said store instruction as executed by said other processor to said store instruction as executed by said self-processor.

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70. The semiconductor integrated circuit as claimed in claim 66, wherein said one kind of said dependence is a read after write dependence, a write after read dependence and an write after write dependence and

10 if said load instruction has been executed by said other processor, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed by said self-processor, from said entry designated by said entry number of said execution history storing unit,

15 if said store instruction has been executed by said other processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said load instruction has been executed by said self-processor, from said entry designated by said entry  
20 number of said execution history storing unit,

if said load instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector stores an instruction execution information, that said load instruction has been executed by said

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self-processor, into said entry designated by said entry number of said execution history storing unit,

if said store instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector stores an instruction execution information, that said store instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed by said other processor into said load instruction as executed by said self-processor, and also detects a possibility of presence of said write after read dependence from said load instruction as executed by said other processor into said store instruction as executed by said self-processor as well as detects a possibility of presence of said write after write dependence from said store instruction as executed by said other processor into said store instruction as executed by said self-processor.

71. The semiconductor integrated circuit as claimed in claim 61, wherein said address converter is adopted to select plural bits of said address inputted and output said plural bits as indicating said entry number.

72. The semiconductor integrated circuit as claimed in claim 71, wherein said address converter is adopted to take an exclusive-OR of said

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selected plural bits and output a value of said exclusive-OR as indicating said entry number.

73. A semiconductor integrated circuit including a detector provided in a self-processor included in a multiple processor system including said self-processor and at least a processor other than said self-processor, and said multiple processor system performing parallel processings in thread units of program, and said detector detecting at least one kind of dependence in address between an instruction included in a thread executed by said self-processor and an instruction included in a thread executed by said other processor, said detector being adopted to detect a possibility of presence of said at least one kind of dependence, as well as said detector detecting at least one kind of dependence in address between instructions included in a thread executed by said self-processor,

wherein if said at least one kind of dependence is present in fact, then said detector detects a possibility of presence of said at least one kind of dependence, and if said at least one kind of dependence is not present in fact, then said detector is allowed to detect said at least one kind of dependence.

74. The semiconductor integrated circuit as claimed in claim 73, wherein said instruction comprises a memory access instruction for access to a memory.



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75. The semiconductor integrated circuit as claimed in claim 74, wherein said detector includes :

an execution history storing unit including a plurality of entry which stores an instruction execution information of whether said memory

5 access instruction has been executed ; and

an address converter for converting an address of said memory access instruction into an entry number of said entry of said execution history storing unit,

10 so that said execution history storing unit stores said instruction execution information into said entry designated by said entry number.

76. The semiconductor integrated circuit as claimed in claim 75, wherein said address converter is adopted to convert a same address of different memory access instructions into a same entry number for allowing  
15 that the same address for said different memory access instructions is stored in the same entry, whereby if said at least one kind of dependence is not present in fact, then said detector is adopted to detect said at least one kind of dependence.

20 77. The semiconductor integrated circuit as claimed in claim 76, wherein only if said memory access instruction has been executed by other processor than said self-processor, and said other processor is to execute a thread which is prior in program sequence to said thread executed by said self-processor, then said address converter is adopted to convert an address

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of said memory access instruction into an entry number of said entry, and said detector reads an instruction execution information, whether or not said memory accesses instruction has been executed, from an entry designated by said entry number.

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78. The semiconductor integrated circuit as claimed in claim 76, wherein if said memory access instruction has been executed by other processor than said self-processor, then said address converter is adopted to convert an address of said memory access instruction into an entry number of said entry, and said detector reads an instruction execution information, whether or not said memory accesses instruction has been executed, from an entry designated by said entry number by referring only a value which has been read out by said memory access instruction which had been executed by other processor executing a thread which is prior in program sequence to said thread executed by said self-processor.

10

15

79. The semiconductor integrated circuit as claimed in claim 76, wherein said memory access instruction comprises either a load instruction or a store instruction.

20

80. The semiconductor integrated circuit as claimed in claim 79, wherein said one kind of said dependence is a read after write dependence, and

if said load instruction has been executed by said self-processor,

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then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector stores an instruction execution information, that said load instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit, and

if said store instruction has been executed by either said self-processor or said other processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said load instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed by either said self-processor or said other processor into said load instruction as executed by said self-processor.

81. The semiconductor integrated circuit as claimed in claim 79, wherein said one kind of said dependence is a write after read dependence, and

if said store instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector stores an instruction execution information, that said store instruction has been executed by said

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self-processor, into said entry designated by said entry number of said execution history storing unit, and

if said load instruction has been executed by either said self-processor or said other processor, then said address converter is adopted to  
5 convert an address of said load instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit,

10 whereby said detector detects a possibility of presence of said write after read dependence from said load instruction as executed by either said self-processor or said other processor into said store instruction as executed by said self-processor.

15 82. The semiconductor integrated circuit as claimed in claim 79, wherein said one kind of said dependence is an write after write dependence, and

if said store instruction has been executed by said other processor, then said address converter is adopted to convert an address of said store  
20 instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit,

if said store instruction has been executed by said self-processor,

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then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed by said self-processor, out from said entry designated by said entry number of said execution history storing unit, as well as said detector stores an instruction execution information, that said store instruction has been executed by said self-processor, into said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said write after write dependence from said store instruction as executed by either said self-processor or said other processor to said store instruction as executed by said self-processor.

83. The semiconductor integrated circuit as claimed in claim 79, wherein said one kind of said dependence is a read after write dependence, a write after read dependence and an write after write dependence and

if said load instruction has been executed by either said self-processor or said other processor, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector reads an instruction execution information, whether or not said store instruction has been executed by said self-processor, from said entry designated by said entry number of said execution history storing unit,

if said store instruction has been executed by either said self-processor or said other processor, then said address converter is adopted to

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convert an address of said store instruction into an entry number, and said detector reads an instruction execution information, whether or not said load instruction has been executed by said self-processor, from said entry designated by said entry number of said execution history storing unit,

5 if said load instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said load instruction into an entry number, and said detector stores an instruction execution information, that said load instruction has been executed by said self-processor, into said entry designated by said entry number of said  
10 execution history storing unit,

if said store instruction has been executed by said self-processor, then said address converter is adopted to convert an address of said store instruction into an entry number, and said detector stores an instruction execution information, that said store instruction has been executed by said  
15 self-processor, into said entry designated by said entry number of said execution history storing unit,

whereby said detector detects a possibility of presence of said read after write dependence from said store instruction as executed by either said self-processor or said other processor into said load instruction  
20 as executed by said self-processor, and also detects a possibility of presence of said write after read dependence from said load instruction as executed by either said self-processor or said other processor into said store instruction as executed by said self-processor as well as detects a possibility of presence of said write after write dependence from said store

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instruction as executed by either said self-processor or said other processor into said store instruction as executed by said self-processor.

84. The semiconductor integrated circuit as claimed in claim 74,  
5 wherein said address converter is adopted to select plural bits of said address inputted and output said plural bits as indicating said entry number.

85. The semiconductor integrated circuit as claimed in claim 84,  
10 wherein said address converter is adopted to take an exclusive-OR of said selected plural bits and output a value of said exclusive-OR as indicating said entry number.